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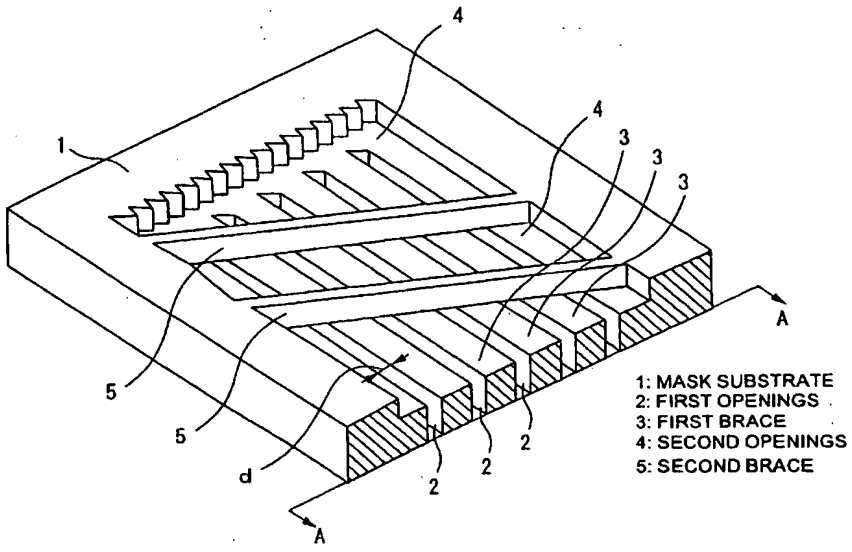
(54) Precision mask for deposition and a method for manufacturing the same, an electroluminescence display and a method for manufacturing the same, and electronic equipment

(57) The present invention aims to provide a precision deposition mask that is easily aligned with a glass substrate in evaporating an emitting layer and the like of an organic EL display, and is strong enough to form an accurate evaporated pattern. The invention also aims to provide a method for easily and accurately manufacturing such a precision deposition mask, an organic EL display and a method for manufacturing the same, and electronic equipment including an organic EL display.

A precision deposition mask according to the invention includes a first brace (3) that is placed in parallel each other at given intervals. The first brace (3) forms portions that define a plurality of first openings (2). The precision deposition mask also includes at least one second brace (5) that is placed on the first brace (3) so as to intersect with the first brace (3). The second brace (5) forms portions that define a plurality of second openings (4). The second brace (5) is joined to the first brace (3) at a point where the second brace (5) intersects with the first brace (3).

FIG. 1



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Description

[0001] The present invention relates to a precision mask for deposition that is mainly used to form a hole transport layer, an emitting layer, and the like of an organic electroluminescence (EL) display, and a method for manufacturing the same. The invention also relates to the organic EL display, a method for manufacturing the same, and electronic equipment having the organic EL display.

[0002] A conventional deposition mask may be formed by wet-etching a single-crystal silicon wafer of surface orientation (100) with potassium hydroxide or the like so as to reduce the thickness of the center of the wafer, and then by dry-etching the wafer to form an opening for deposition corresponding to each pixel of the organic EL display (see JP 2001-185350 A, for example). The deposition mask corresponds to the precision mask for deposition according to the invention.

[0003] A conventional mask for evaporation may be formed by wet-etching a single-crystal silicon wafer of surface orientation (100) with potassium hydroxide or the like so as to reduce the thickness of part of the wafer, and by further wet-etching the wafer with potassium hydroxide or the like to form an evaporated pattern (an opening) (see JP 4-236758 A, for example). The mask for evaporation corresponds to the precision mask for deposition according to the invention.

[0004] A conventional precision mask for deposition having a single-crystal silicon wafer that is used for an organic EL display may include a plurality of elongated openings that are several dozen micrometers wide aligned as shown in FIG. 10. The openings make it possible to form pixels at a time that are arranged lengthwise and each emit either red, green, or blue light.

[0005] The conventional deposition mask having an opening for deposition corresponding to each pixel of the organic EL display (see JP 2001-185350 A, for example) involves the following problem. It is necessary to align the mask for deposition with a glass substrate to which an emitting layer is evaporated within a tolerance of +/- five (5) micrometers both lengthwise and crosswise in a vacuum evaporation room. This hinders productivity.

[0006] The conventional mask for evaporation that is formed by wet-etching a single-crystal silicon wafer of surface orientation (100) to form an opening (see JP 4-236758 A, for example) also involves the following problem. If a plurality of elongated openings that are several dozen micrometers wide is aligned as shown in FIG. 10, part of the silicon wafer that is between two openings is too weak to bear up. Thus, an evaporated wafer is not accurately patterned.

[0007] In consideration of these problems, the invention aims to provide a precision mask for deposition (simply referred to as "deposition mask" hereinafter) that is easily aligned with a glass substrate in evaporating an emitting layer and the like of an organic EL display, and is strong enough to form an accurate evaporated pattern. The invention also aims to provide a method for easily and accurately manufacturing such a deposition mask, an organic EL display and a method for manufacturing the same, and electronic equipment including an organic EL display.

[0008] This object is achieved by a precision deposition mask as claimed in claim 1, a method as claimed in claim 7 and their preferred embodiments as claimed in the dependent claims.

[0009] According to the invention, the second brace, which defines the second openings, serves as reinforcement for the first brace, which defines the first openings. The first openings are several dozen micrometers wide and several centimeters long, which are elongated in shape. Since the second brace is joined to the first brace and serves as reinforcement, the first brace does not bend. As a result, an accurate evaporated pattern can be provided. In addition, since the first openings are elongated in shape, the deposition mask is easily aligned with the glass substrate when evaporating the emitting layer etc. as described in greater detail below.

[0010] Since, preferably, the first brace and the second brace are formed to be joined to the mask substrate, the deposition mask according to the invention provides high accuracy and rigidity.

[0011] With the mask substrate that is preferably made of single-crystal silicon, the deposition mask according to the invention provides high accuracy and rigidity. Moreover, the deposition mask is easily manufactured by wet etching.

[0012] Since at least one of the side surfaces of the first brace and the second brace is preferably of surface orientation (111), the deposition mask according to the invention is easily manufactured by anisotropic-etching the mask substrate that is made of single-crystal silicon by potassium hydroxide or the like, when forming the first openings and the second openings.

[0013] According to one embodiment of the invention, the second brace, which defines the second openings of the mask substrate, serves as reinforcement for the first brace, which defines the first openings of the mask substrate. Since the second brace is joined to the first brace and serves as reinforcement, the first brace does not bend. As a result, an accurate evaporated pattern can be provided. Since both of the side surfaces of the first brace and the second brace are of surface orientation (111), the deposition mask is easily manufactured by wet-etching a silicon wafer by potassium hydroxide or the like, when forming the first openings and the second openings.

[0014] The preferred embodiment of the invention provides a deposition mask that provides higher accuracy by using a single-crystal silicon wafer whose oxygen concentration is low, which can avoid developing a crystal defect when the mask substrate reaches a high temperature in manufacturing the deposition mask.

[0015] In the method according to the invention, the

etching protective film is formed on both the surface (front side) and the back (rear side) of a single-crystal silicon wafer. The single-crystal silicon wafer is then patterned by photolithography or the like and removed in parts that are patterned, which is to be the openings by anisotropic etching. With the method including these steps, a deposition mask that can form an accurate evaporated pattern is easily and accurately manufactured.

[0016] If the temperature of the mask substrate is from 500 to 800 °C, it is preferred to quickly pass through this temperature range in which a crystal defect is most likely to develop by cooling the mask substrate at an average cooling rate of at least 3 °C per minute makes. Thus the deposition mask according to the invention provides higher accuracy.

[0017] An EL display according to the invention includes the deposition mask mentioned above.

[0018] Since the EL display according to the invention is manufactured with the deposition mask, which provides high accuracy and is easily aligned with the glass substrate when evaporating the emitting layer etc. as described above, the EL display offers high quality with an accurate evaporated pattern.

[0019] A method for manufacturing the EL display according to the invention includes the step of placing the deposition mask mentioned above at a predetermined position on the glass substrate so as to form an EL layer.

[0020] Since the EL display according to the invention is manufactured with the deposition mask, which provides high accuracy and is easily aligned with the glass substrate when evaporating the emitting layer etc. as described above, the EL display offers high quality with an accurate evaporated pattern.

[0021] Furthermore, the method for manufacturing the EL display is simple, which can reduce cost.

[0022] Electronic equipment having the EL display according to the invention includes an EL layer that is manufactured with the deposition mask mentioned above.

[0023] The electronic equipment having the EL display according to the invention includes the EL display, which offers high quality with an accurate evaporated pattern. Furthermore, since the method for manufacturing the EL display is simple, cost can be reduced.

[0024] Preferred embodiments of the invention will be described in detail below with reference to the attached drawings.

FIG. 1 is a diagram schematically showing a deposition mask according to a first embodiment of the invention.

FIG. 2 is a cross-section view of an electrode part of an organic EL display according to the invention.

FIG. 3 is a diagram showing a method for manufacturing a deposition mask according to the invention.

FIG. 4 is a chart showing temperature changes by thermal oxidation shown in FIG. 3A.

FIG. 5 is a drawing showing a pattern on the surface of the mask substrate.

FIG. 6 is a drawing showing a pattern on the back of the mask substrate.

FIG. 7 is a comparison chart of electrode configurations for an organic EL display.

FIG. 8 is a drawing showing the spatial relationship of the glass substrate and the deposition mask when using evaporation.

FIG. 9 is a diagram showing electronic equipment according to a fifth embodiment of the invention.

FIG. 10 is a drawing showing a conventional deposition mask.

First Embodiment

[0025] FIG. 1 is a diagram schematically showing a deposition mask according to a first embodiment of the invention. The mask is cut along the A-A line in FIG. 1, and portions of the mask not shown in this diagram are formed in the same pattern. A mask substrate 1 is provided by cutting a single-crystal silicon wafer into a rectangle. Facing the back (back side) of the mask substrate 1, a first brace 3 is provided. In this diagram the first brace 3 includes a plurality of braces that are placed in parallel to each other at given intervals. The intervals form a plurality of first opening 2. Facing the surface (front side) of the mask substrate 1, a second brace 5 is provided. In this diagram the second brace 5 includes a plurality of braces that form a plurality of second openings 4. The first brace 3 and the second brace 5 are formed to be joined to the mask substrate 1, which is made of single-crystal silicon. A method for manufacturing them is described below in a third embodiment. At a point where the first brace 3 intersects the second brace 5, the upper surface of the first brace 3 is joined to the lower surface of the second brace 5. When evaporating an organic EL material, the first brace 3 is in contact with the evaporated material.

[0026] FIG. 1 schematically shows the deposition mask. In general, the width "d" of the first openings 2 is from several micrometers to several dozen micrometers. The first brace 3 is about twice as wide as the first openings 2. The length of the first openings 2 is, in general, from several centimeters to several dozen centimeters. Thus the first openings 2 are elongated in shape.

[0027] The deposition mask according to the first em-

bodiment shown in FIG. 1 is formed by cutting the mask substrate 1 out of a single-crystal silicon wafer of surface orientation (110). The side surfaces of the first brace 3 are perpendicular (111) to the surface orientation (110) of the mask substrate. The side surfaces of the second brace 5 intersect the side surfaces of the first brace 3, and are also perpendicular (111) to the surface orientation of the mask substrate. The side surfaces of the braces face neither the surface and the back of the mask substrate 1 for the side surfaces of the braces 5. The deposition mask is provided by, for example, cutting a single-crystal silicon wafer of surface orientation (110) into a rectangle, which is to be the mask substrate 1. The first openings 2 and the second openings 4 are easily formed by anisotropic etching with potassium hydroxide or the like. A method for manufacturing the deposition mask according to the invention is described below in greater detail in a second embodiment.

[0028] It should be noted that although the side surfaces of the first brace 3 and the second brace 5 are perpendicular to the surface of the mask substrate 1 in the first embodiment, it is not always necessary to form the side surfaces of the braces perpendicular to the surface of the mask substrate. For example, if the first brace 3 is formed so as to have a trapezoidal cross-section, the first openings 2 have an inverted trapezoidal cross-section. This makes it possible to evaporate a material with a wide angle.

[0029] Furthermore, the first brace 3 may be made of a different material from that of the second brace 5.

[0030] FIG. 2 is a cross-section view of an electrode part of an organic EL display that is an example of an EL display manufactured with the deposition mask according to the first embodiment of the invention. The diagram shows that a glass substrate 6 is provided at the bottom. On this substrate, a TFT wiring layer 7, a planarizing insulating film 8, and an ITO layer 9 are deposited in this order. ITO stands for indium thin oxide that serves as an anode to apply an electric current to pixels. Then a silicon oxide layer 10 is deposited on a part that emits no light around each pixel. Subsequently, a hole transport layer 11, an emitting layer 12, and an electron injection layer 13, all of which form an EL layer and are made of an organic EL material, are deposited by, for example, vacuum evaporation. On top of them, an ITO layer 14 that serves as a cathode and a transparent sealant film 15 are deposited. The deposition mask shown in FIG. 1 is mainly used as a mask for evaporating the hole transport layer 11, the emitting layer 12, and the electron injection layer 13. In addition, the mask can be used as a mask for sputtering when forming the ITO layer 9 by sputtering. The EL layer may include a hole injection layer and the like if any, as well as the hole transport layer 11, the emitting layer 12, and the electron injection layer 13.

[0031] The deposition mask (the mask substrate 1) according to the first embodiment includes the second brace 5 that is joined to the first brace 3. Therefore, the mask is strong enough to bear up and forms an accurate evaporated pattern. Also as regards the deposition mask according to the first embodiment, as shown in a fourth embodiment described later in detail, the emitting layer 12 etc. are deposited while the first openings 2, which are elongated in shape, are aligned with a portion on the glass substrate 6 where pixels are formed. This makes it easy to align the mask substrate 1 with the glass substrate 6, which can improve production efficiency.

[0032] Also according to the first embodiment, the side surfaces of the first brace 3 and the second brace 5 are perpendicular (111) to the mask substrate 1. This makes it easy to form the deposition mask by anisotropic etching with potassium hydroxide or the like. In addition, since the side surfaces of the first brace 3 are perpendicular to the mask substrate 1, the first openings 2 can be formed precisely.

Second Embodiment

[0033] FIG. 3 shows cross-section views of the mask substrate 1 illustrating a method for manufacturing the deposition mask according to the first embodiment. First, the mask substrate 1 is provided by cutting a single-crystal silicon wafer of surface orientation (110) into a rectangle. After cleaning the mask substrate 1, an etching protective film 17 that is made of silicon oxide (SiO_2) is formed by thermal oxidation so as to surround the mask substrate 1 (see FIG. 3A). The etching protective film 17 may be obtained by forming a silicon nitride film by chemical vapor deposition (CVD) or forming a gold-chrome alloy film by sputtering instead of by forming a silicon oxide film by thermal oxidation.

[0034] According to the second embodiment, single-crystal silicon whose oxygen concentration is $1.7*10^{18}$ atm/cm^3 or below is used for the mask substrate 1. If the temperature of the mask substrate 1 is from 500 to 800 °C after forming the etching protective film 17 by thermal oxidation, the mask substrate 1 is cooled at an average cooling rate of at least 3 °C per minute.

[0035] FIG. 4 is a chart showing an example of temperature changes in forming the etching protective film 17 by thermal oxidation as shown in FIG. 3A. When the temperature reaches 800 °C, the temperature is increased up to 1100 °C by supplying oxygen to a thermal oxidation room. When the temperature reaches 1100 °C, steam is supplied to the thermal oxidation room in order to accelerate thermal oxidation. When thermal oxidation is completed after keeping the temperature of 1100 °C for a while, nitrogen is supplied in order to stabilize the etching protective film 17. Then, the temperature is lowered from 1100 °C.

[0036] If the temperature of the mask substrate 1 is from 500 to 800 °C, the mask substrate 1 is cooled at an average cooling rate of at least 3 °C per minute. This is because the possibility of developing a crystal defect of single-crystal silicon is highest in this temperature

range. If the mask substrate 1 has a crystal defect, openings may not be accurately formed by anisotropic etching. Developing such a crystal defect can be avoided by passing through this temperature range quickly.

[0037] The mask substrate also reaches a temperature of 500 °C or higher when the etching protective film 17 of silicon nitride is formed by CVD or the etching protective film 17 of gold-chrome alloy by sputtering instead of thermal oxidation. Also in these cases, if the temperature of the mask substrate is from 500 to 800 °C, developing a crystal defect can be avoided by cooling the mask substrate at an average cooling rate of at least 3 °C per minute.

[0038] Furthermore, by using single-crystal silicon whose oxygen concentration is $1.7*10^{18}$ atm/cm^3 or below for the mask substrate 1, developing a crystal defect caused by a higher-temperature process can be avoided.

[0039] Next, configurations corresponding to the first openings 2 that are defined by the first brace 3 are patterned on the back of the mask substrate 1 where the etching protective film 17 is formed. Also, configurations corresponding to the second openings 4 that are defined by the second brace 5 are patterned on the surface of the mask substrate. The configurations are patterned by photolithography on portions other than the openings. FIG. 5 shows a pattern on the surface of the mask substrate 1, while FIG. 6 shows a pattern on the back of the mask substrate 1. Photolithography is performed in the hatched areas in FIGs. 5 and 6. The arrows "J" and "K" in FIGs. 5 and 6 are in the direction of (111). Then the mask substrate 1 on which the configurations are patterned is etched by a solution of hydrofluoric acid and ammonium fluoride so as to remove the etching protective film in parts to be the openings (see FIG. 3B). Here, a part to be an alignment mark 20 that is necessary when setting a position of evaporating the emitting layer 12 etc. of the organic EL display that is mentioned in the first embodiment is also etched.

[0040] The mask substrate 1 that is etched as shown in FIG. 3B is then anisotropic-etched with a potassium hydroxide solution so as to form the first openings 2 and the second openings 4 (see FIG. 3C). By wet etching with potassium hydroxide, part of the mask substrate that is not covered by silicon oxide is etched accurately with the side surfaces of surface orientation (111). When the organic EL display includes a semiconductor, organic alkaline solutions such as a tetramethylammonium hydroxide solution are preferably used for etching, instead of the potassium hydroxide solution. This is because the semiconductor may be contaminated by potassium. Also in this case, anisotropic etching can be performed as is the case with potassium hydroxide.

[0041] Finally, the etching protective film 17 that remains on the mask substrate 1 shown in FIG. 3C is removed by a buffer hydrogen fluoride solution or the like. As a result, the deposition mask is formed (see FIG. 3D).

[0042] By performing anisotropic etching after forming the etching protection film, the method for manufacturing a deposition mask according to the second embodiment makes it possible to easily and accurately manufacture a precision deposition mask that is strong enough to form an accurate evaporated pattern as shown in FIG. 1. Moreover, by cooling the mask substrate 1 at an average cooling rate of 3 °C per minute if the temperature is from 500 to 800 °C so as to quickly pass through this temperature range in which a crystal defect is likely to develop, and by using single-crystal silicon whose oxygen concentration is $1.7*10^{18}$ atm/cm^3 or below for the mask substrate 1, the method makes it possible to avoid developing a crystal defect and thereby to accurately perform anisotropic etching.

Third Embodiment

[0043] The electrode part of an organic EL display whose EL layer is manufactured with the deposition mask according to the first embodiment of the invention has a cross section as shown in FIG. 2. An electrode configuration as viewed from the surface side of an EL display according to a third embodiment is called vertical stripes. Three major electrode configurations for an organic EL display are described below.

[0044] FIG. 7 is a comparison chart of the electrode configurations for an organic EL display in terms of the difficulty of thin-film transistor (TFT) wiring, image display quality, and character display quality. TFT wiring means general wiring for driving an organic EL display. It controls switching on and off of each pixel. Electrode configurations have an important influence on display quality, in particular, as regards a full-color low-molecular organic EL display. As shown in FIG. 7, a configuration called delta configuration has the disadvantages of complicated TFT wiring and low character display quality. A configuration called square configuration also has the disadvantages of rather complicated TFT wiring and high cost. In the configuration called vertical stripes, pixels whose width is 20 micrometers and length is 60 micrometers, for example, are arranged. An organic EL display of vertical stripes requires simple TFT wiring and low cost, while it provides high image and character display quality.

[0045] Since the deposition mask shown in FIG. 1 includes the first openings 2 that are elongated in shape, it is suitable for manufacturing the organic EL display of vertical stripes.

[0046] Since the EL display according to the third embodiment is manufactured with the deposition mask according to the first embodiment shown in FIG. 1, which is sufficiently strong, the display provides high precision with accurate pixel patterns. In addition, since the display adopts the vertical-stripe pixel configuration, it requires simple TFT wiring and low costs, while it provides high image and character display quality.

Fourth Embodiment

[0047] FIG. 8 shows the spatial relationship of the glass substrate 6 and the deposition mask (the mask substrate 1) when vacuum-evaporating the EL layer to the organic EL display shown in FIG. 2 in manufacturing the organic EL display. The organic EL display shown in FIG. 8 adopts the vertical-stripe pixel configuration. The TFT wiring layer 7, the planarizing insulating film 8, the ITO layer 9, and the silicon oxide layer 10 are deposited on the glass substrate 6 (see Fig. 2). The mask substrate 1 (not shown in the diagram) is provided in a manner that its back (the side on which the first openings 2 are formed) is in contact with the glass substrate 6. As shown in FIG. 8, the first openings 2 are aligned with vertical lines of pixels. In addition, an evaporation source is on the side of the mask substrate 1. The first openings 2 are designed so as to provide an opening every three vertical pixel lines and evaporate pixels that emit the same color at a time. In other words, red pixels 21 R, green pixels 21 G, and blue pixels 21 B are each arranged lengthwise. Pixels of a desired color are evaporated only by moving the mask substrate 1 to the line of pixels of the color and aligning the mask substrate 1 with the glass substrate 6.

[0048] Above the mask substrate 6, the silicon oxide layer 10, which is an insulator, is deposited on a part that emits no light around each pixel as shown in FIG. 2. Thus, even if the EL layer is formed over the first openings 2, pixels are separated from one another. When vacuum-evaporating the emitting layer 12 etc., it is therefore sufficient to pay attention only to lateral alignment accuracy and not to longitudinal alignment accuracy when aligning the mask substrate 1 with the glass substrate 6. Since the mask substrate 1 is aligned with the glass substrate 6 in a vacuum evaporation room, achieving high longitudinal and alignment accuracies requires time and money, and reduces production efficiency as a result.

[0049] However, using the deposition mask (the mask substrate 1) shown in FIG. 1 makes it easy to align the mask substrate 1 with the glass substrate 6, which improves production efficiency. In addition, since the first openings 2 are elongated in shape, the mask is suitable for manufacturing the organic EL display of vertical-stripe pixel configuration.

[0050] In order to reduce the need for high longitudinal alignment accuracy as mentioned above, one option is to use such a mask for evaporation as the one shown in FIG. 10. The problem here is that braces between elongated openings are several dozen micrometers wide in general, which are too weak to bear up. This means it is difficult to make an accurate evaporated pattern. The deposition mask shown in FIG. 1, however, includes at least one of the second brace 5, which is joined to the first brace 3. Thus, the first brace 3 does not easily bend.

[0051] The emitting layer 12 etc. may not be evaporated evenly because of the second brace 5. To solve this problem, thickness distribution is evenly balanced within a pixel by rotating the glass substrate 6 and the mask substrate 1 together in a vacuum evaporation room and moving an evaporation source as required.

[0052] Furthermore, as regards the method for manufacturing an EL display according to the fourth embodiment, the emitting layer 12 etc. are deposited while the first openings 2, which are elongated in shape, are aligned with a portion on the glass substrate 6 where pixels are formed. This makes it easy to align the mask substrate 1 with the glass substrate 6, which can improve production efficiency. Moreover, since the deposition mask (the mask substrate 1) according to the first embodiment includes the second brace 5, the mask is strong enough to bear up and forms an accurate evaporated pattern.

Fifth Embodiment

[0053] FIG. 9 is a diagram showing electronic equipment according to a fifth embodiment of the invention. FIG. 9A shows an example of the EL display according to the invention used as a display panel of a cellular phone. FIG. 9B shows an example of the EL display according to the invention used as a display panel of a digital panel. Other examples in which the EL display according to the invention can be used as a display include game machines and computers.

Claims

1. A precision deposition mask, comprising:

   a first brace having first brace portions (3) that are placed in parallel to each other at given intervals;
   the first brace portions (3) defining a plurality of first openings (2);
   a second brace having second brace portions (5) that are placed on the first brace so as to intersect the first brace portions (3);
   the second brace portions (5) defining a plurality of second openings (4); and
   the second brace being joined to the first brace where the second brace portions (5) intersect the first brace portions (3).

2. The mask according to Claim 1, further comprising:

   a mask substrate (6), wherein the first brace and the second brace are formed to be joined to the mask substrate (6).

3. The mask according to Claim 2, wherein the mask substrate (6) is made of single-crystal silicon.

4. The mask according to Claim 3, wherein at least one of side surfaces of the first brace portions (3) and the second brace portions (5) is of surface orientation (111).

5. The mask according to Claim 3 or 4,
wherein the mask substrate (6) is made of single-crystal silicon of surface orientation (110);
side surfaces of the first brace portions (3) have surface orientation (111) being perpendicular to surface orientation (110) of the mask substrate (6); and
side surfaces of the second brace portions (5) have surface orientation (111) being perpendicular to surface orientation (110) of the mask substrate (6).

6. The mask according to any one of Claims 3 to 5, wherein the oxygen concentration of the mask substrate (6) is $1.7*10^{18}$ atm/cm^3 or below.

7. A method of manufacturing the precision deposition mask according to any one of Claims 1 to 6, the method comprising the steps of:

a) forming an etching protective film (17) on the mask substrate (6) that is made of single-crystal silicon;
b) patterning configurations corresponding to the plurality of first openings (2), defined by first brace portions (3) on the back of the mask substrate (6), on the etching protective film (17);
c) patterning configurations corresponding to the plurality of second openings (4), defined by the second brace portions (5) on the surface of the mask substrate (6), on the etching protective film (17);
d) removing the etching protective film (17) in parts that are patterned; and
e) forming the first openings (2) and the second openings (4) by etching.

8. The method according to Claim 7, wherein step a) further comprises the steps of:

a1) heating the mask substrate (6) up to 500 °C or higher;
a2) cooling the mask substrate (6); and
a3) cooling the mask substrate (6) at an average cooling rate of at least 3 °C per minute in the temperature range from 500 to 800 °C.

9. The method according to Claim 8, wherein step a) further comprises the step of:

forming the etching protective film by thermal oxidation.

10. Use of the precision deposition mask according to any one of Claims 1 to 6 for evaporating an electroluminescence layer (11; 12; 13) of an electroluminescence display.

11. An electroluminescence display comprising:

an electroluminescence layer that is formed with the precision deposition mask according to any one of Claims 1 to 6.

12. Electronic equipment, comprising:

the electroluminescence display according to Claim 11.

FIG. 1

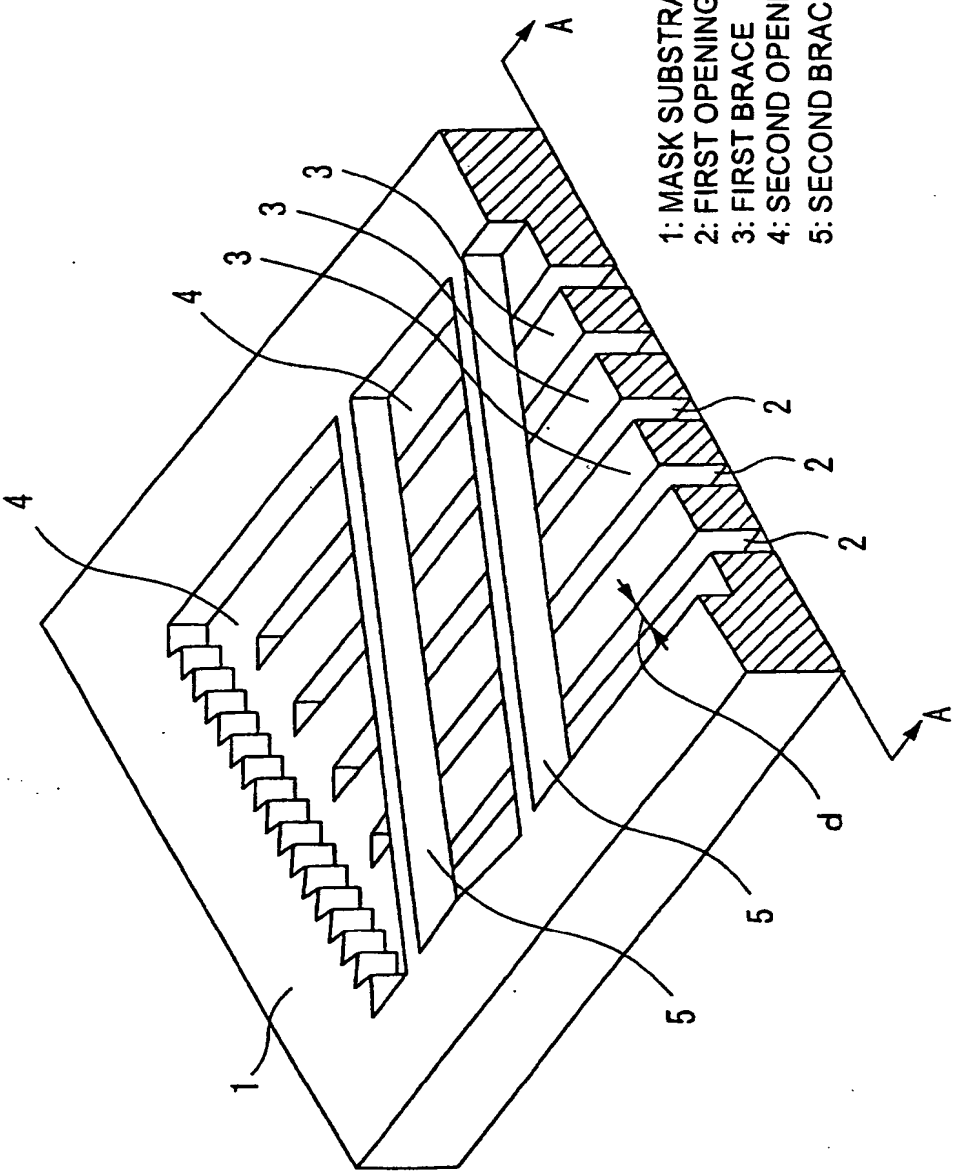

FIG. 2

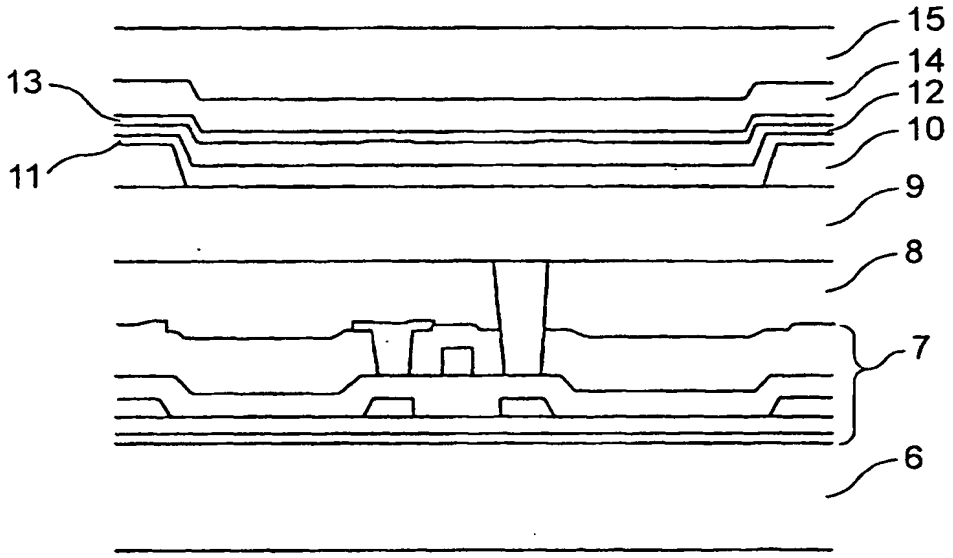

FIG. 3 A

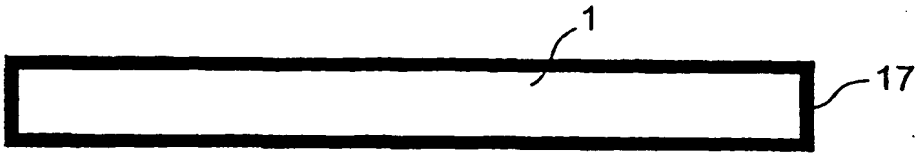

FIG. 3 B

FIG. 3 C

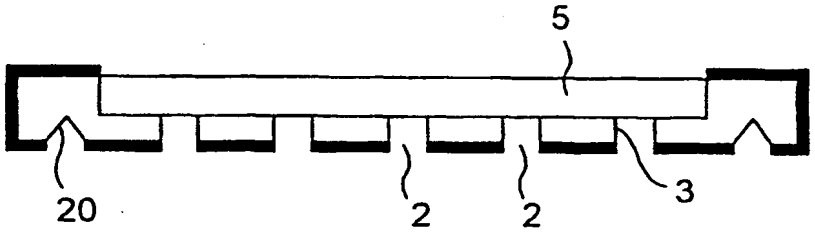

FIG. 3 D

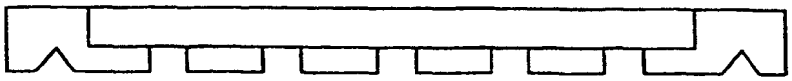

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FIG. 4

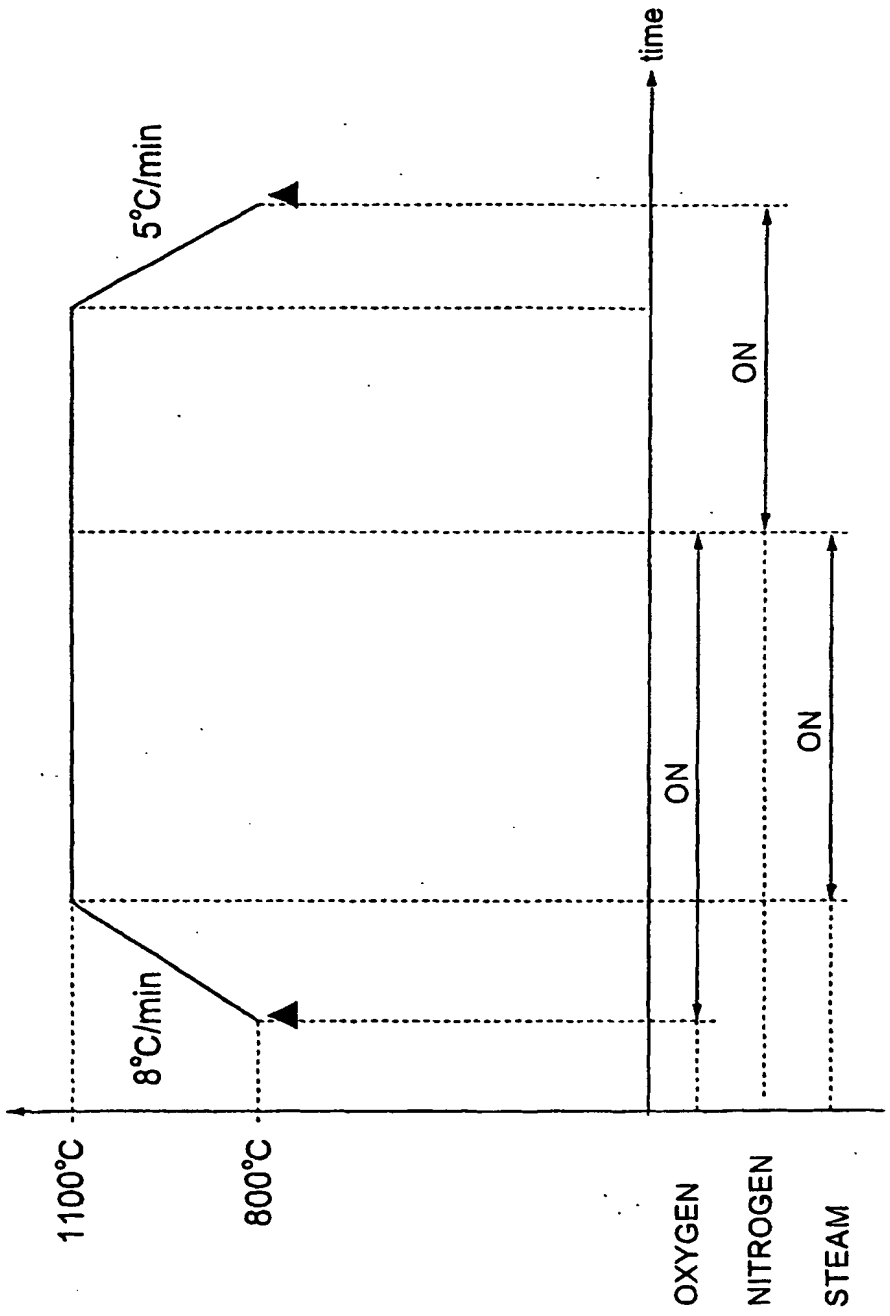


FIG. 5

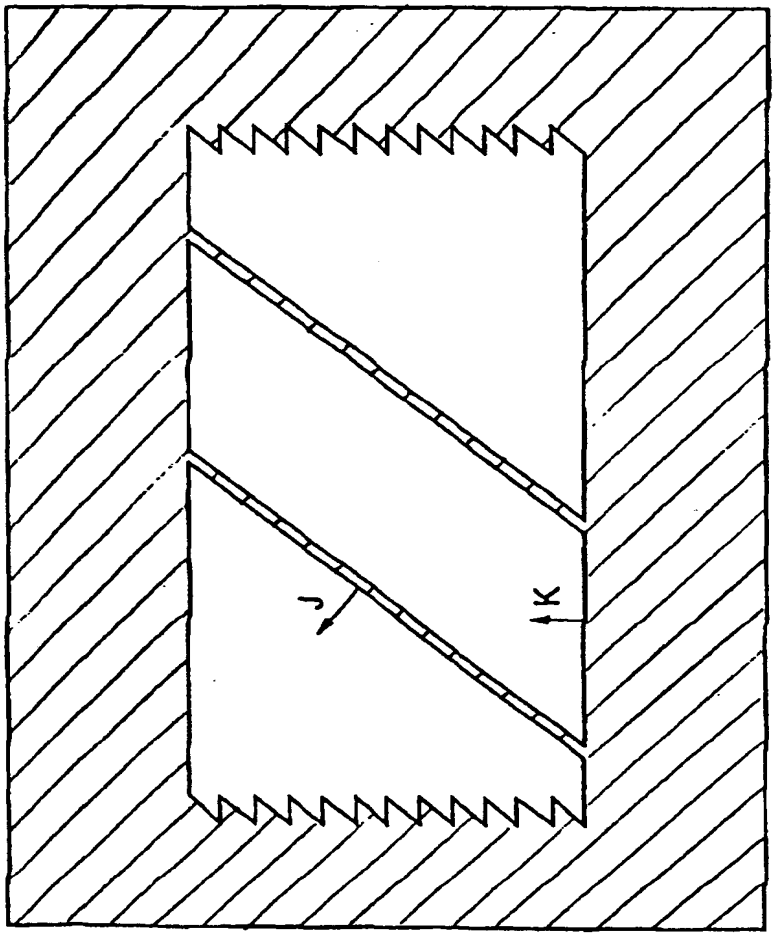


FIG. 6

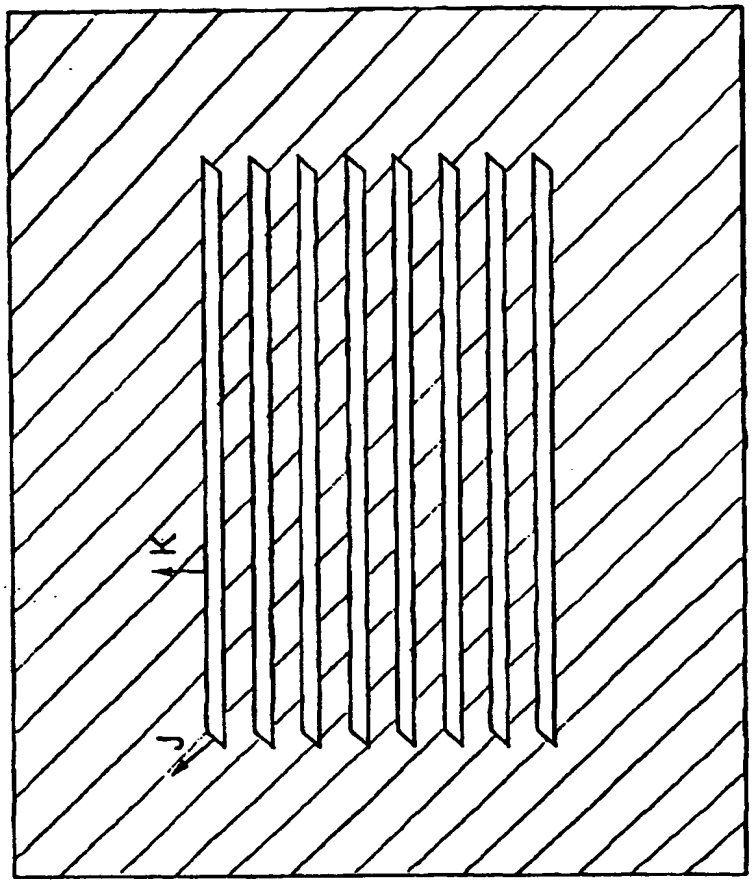


FIG. 7

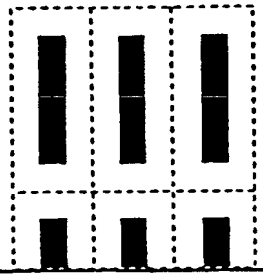
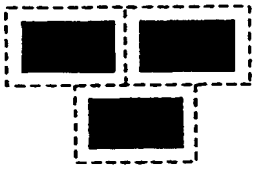
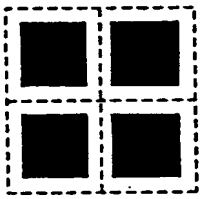
PIXEL CONFIGURATION	SCHEMATIC DIAGRAM	TFT WIRING	IMAGE DISPLAY QUALITY	CHARACTER DISPLAY QUALITY
VERTICAL STRIPES		SIMPLE	○	○
DELTA CONFIGURATION		DIFFICULT	○	△
SQUARE CONFIGURATION		DIFFICULT	○	○

FIG. 8

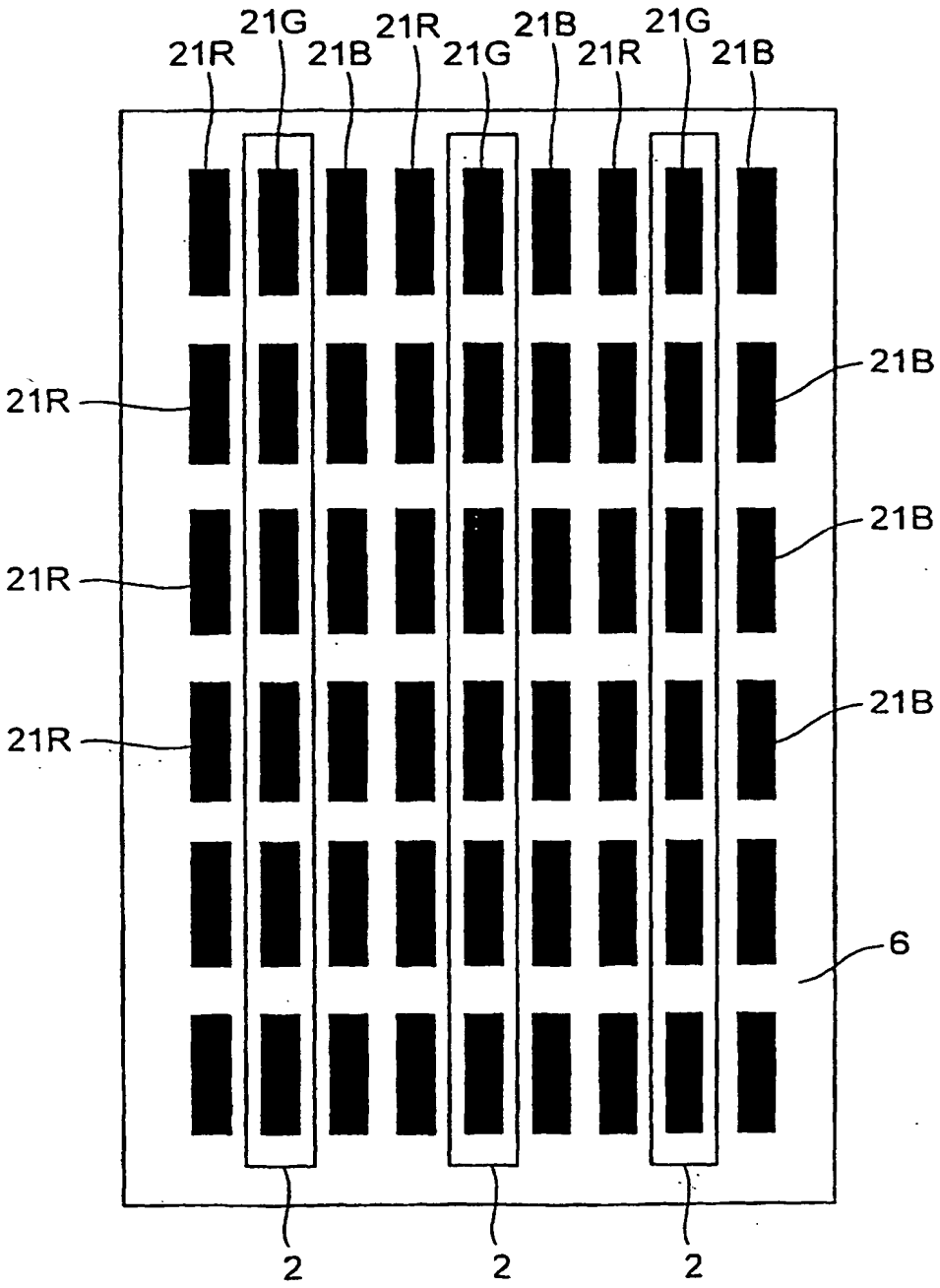


FIG. 9 A

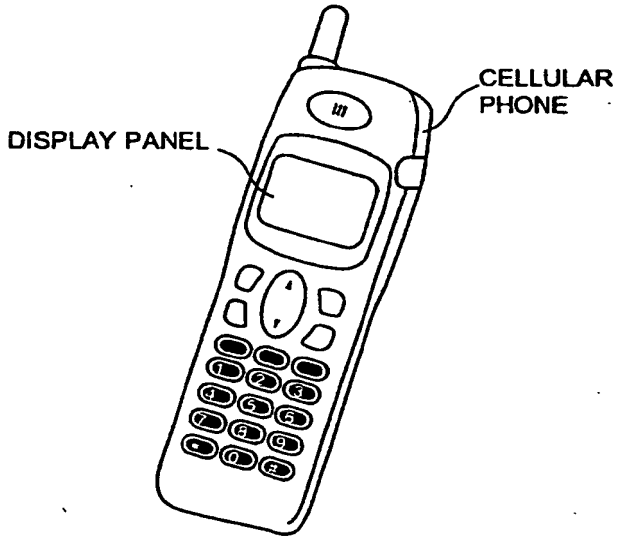


FIG. 9 B

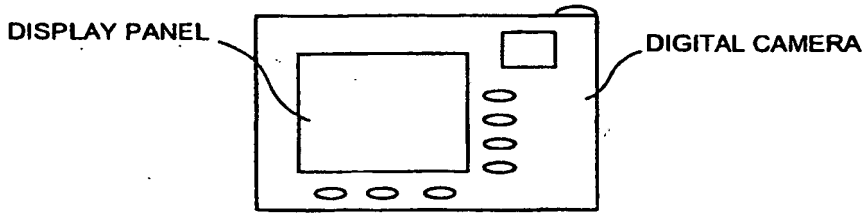
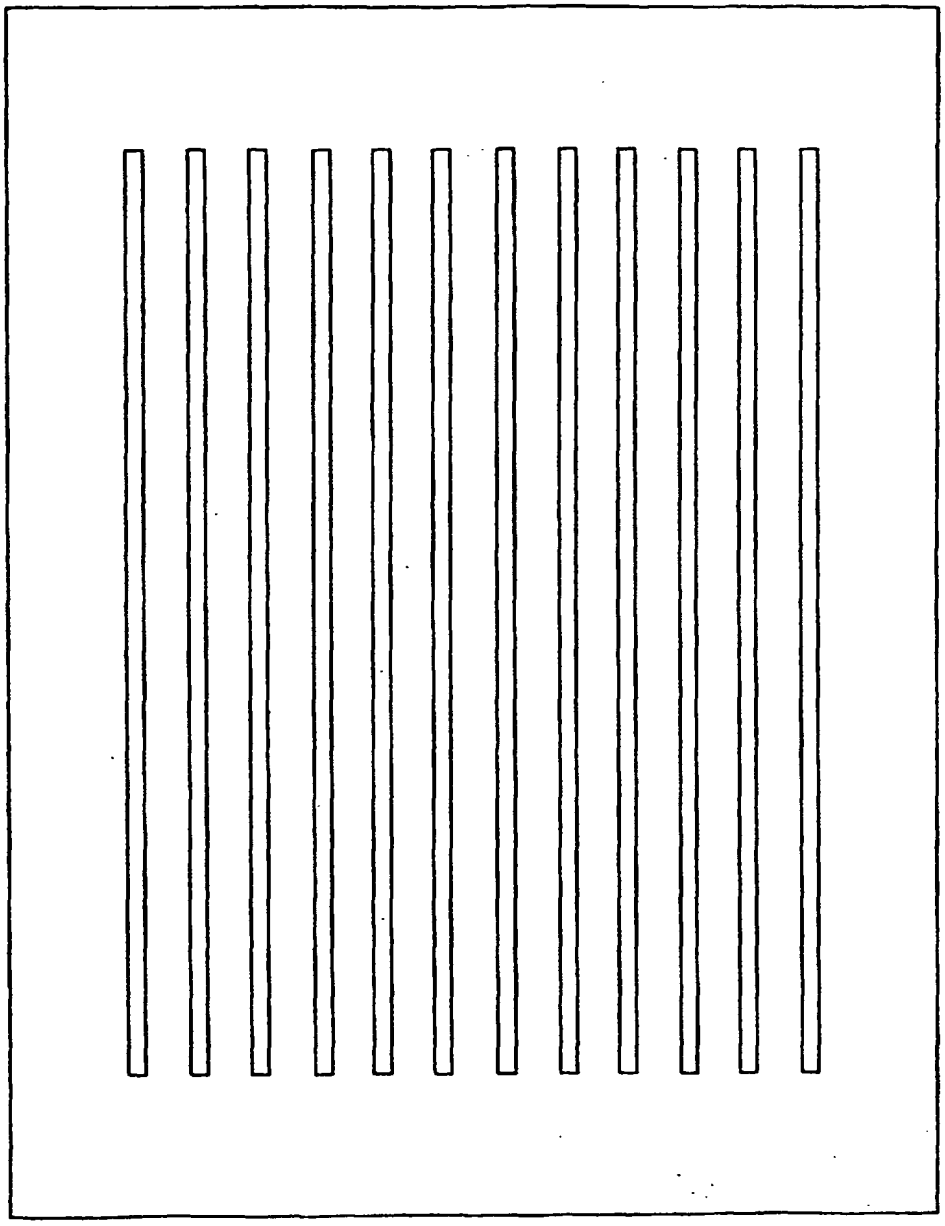


FIG. 10



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 04 00 0271

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 2002/111035 A1 (KAMISUKI SHINICHI ET AL) 15 August 2002 (2002-08-15) * figures 23,24 *	11,12	H05B33/08 H01L27/15 C23C14/04 C23C16/04
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MUNICH	26 April 2004	Kiliaan, S

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

Application No:	GB0410364.4	**Examiner:**	Helen Edwards
Claims searched:	All	**Date of search:**	16 August 2004

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A,E	-	EP1441572 A1 (SEIKO EPSON CORPORATION)
A	-	EP1274130 A2 (LG ELECTRONICS)

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Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^{W} :

G5C; H1K

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G09G; H01L; H05B

The following online and other databases have been used in the preparation of this search report

EPODOC, JAPIO, WPI